Remarks

The non-final Office Action dated March 24, 2008 listed the following rejections: claims 7 and 14 stand rejected under 35 U.S.C. § 112(2); claims 1-14 stand rejected under 35 U.S.C. § 102(b) over Buckland (U.S. Patent No. 4,744,081); claim 15 stands rejected under 35 U.S.C. § 103(a) over Buckland in view of Giorgetta (U.S. Patent No. 7,035,292); claims 1-2, 5, 7-9, 12 and 14 stand rejected under 35 U.S.C. § 103(a) over Surie (U.S. Patent No. 4,675,886) in view of O'Connor (U.S. Patent No. 5,005,191); claims 3-4 and 10-11 stand rejected under 35 U.S.C. § 103(a) over Surie and O'Connor reference and in further view of Bruekheimer (U.S. Patent No. 5,367,544); claim 15 stands rejected under 35 U.S.C. § 103(a) over Surie and O'Connor in further view of Giorgetta.

Applicant respectfully traverses the § 112(2) rejection of claims 7 and 14 because these claims do particularly point out and distinctly claim the invention. The Office Action asserts that it is unclear if the term "blocking" modifies an input to the clock means, an output of the clock means, or an internal function of the clock means. Thus, the Office Action appears to be equating the breadth of the claims to indefiniteness. Such an assertion is contrary to M.P.E.P. § 2173.04 because the "(b)readth of a claim is not to be equated with indefiniteness." *See In re Miller*, 441 F.2d 689 (CCPA 1971). Applicant submits that the scope of claims 7 and 14 would be clear to the skilled artisan, as such, these claims are definite in compliance with§ 112(2). Moreover, Applicant submits that the amendments to claims 7 and 14 render the § 112(2) moot. Accordingly, Applicant requests that the § 112(2) rejection of claims 7 and 14 be withdrawn.

Applicant respectfully submits that the § 102(b) rejection of claims 1-14 and § 103(a) rejection of claim 15 (each of which is based on the Buckland reference) cannot stand because the cited portions of Buckland do not correspond to the claimed invention which includes, for example, aspects directed to preventing one of the first clock pulses that clock the serial portion of the shift register from reaching the second clock circuitry, which clocks the parallel portion of the shift register, when a frameheader is not detected. The cited portions of Buckland do not teach preventing any pulses of the serial clock signal on line 26, which clocks shift register 16, from reaching divider 20, which produces the clock signal on line 28 that clocks latch 18. *See, e.g.,* Figure 1 and Col. 2:40-66. Instead Buckland teaches changing the number by which divider 20 divides the clock signal on line

26 when the frame word is not detected. *See, e.g.,* Col. 3:21-40. Thus, the cited portions of Buckland do not correspond to the claimed invention. Accordingly, Applicant requests that the § 102(b) rejection of claims 1-14 and § 103(a) rejection of claim 15 based on the Buckland reference be withdrawn.

Applicant respectfully traverses the § 103(a) rejections of claims 1-15 (based on the Surie reference) because the modification of Surie proposed by the Office Action undermines a stated purpose of Surie. According to M.P.E.P. § 2143.01, "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. " *See also In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984). In this instance the Office Action proposes to modify Surie to replace shift register 11 (*see, e.g.,* Figure 1) with "one having more bit positions than contained in a frame". *See* page 9:10-15 of the instant Office Action. However, a stated purpose of Surie is to implement frame synchronization in a simpler and faster manner by using a shift register that is smaller than the frame size and by only shifting selected bits of the frame into the shift register (*e.g.,* Surie reduces the amount of data stored in the shift register). *See, e.g.,* Col. 1:30-65 and Col. 2:11-16. For example, Surie teaches that a frame consists of eight sectors of 20 bits each and that shift register 11 is controlled by clock signal H1, which causes only every 20^{th} bit to be shifted into the shift register 11. *See, e.g.,* Figure 1 and Col. 4:35-51. As such, Applicant submits that the Office Action's proposed modification of Surie would undermine Surie's stated purpose of implementing frame synchronization in a simpler and faster manner that uses a smaller shift register. Accordingly, there would be no motivation for the skilled artisan to modify Surie in the manner proposed by the Office Action.

Moreover, the Office Action's proposed modification of Surie would not "lead to faster synchronization" as asserted by the Office Action. The Office Action's proposed modification of Surie would result in shift register 11 "having more bit positions than contained in a frame"; however, the bits of a frame would still be read into shift register 11 responsive to clock signal H1 (*i.e.,* only every 20^{th} or 21^{st} bit of a frame is read into the shift register). *See, e.g.,* Figure 1 and Col. 4:35-51. Thus, the bits of a frame would still be read into Surie's shift register 11 (which would simply be substantially larger) at

the same speed. Accordingly, the Office Action's proposed modification would not result in faster synchronization.

In view of the above, the § 103(a) rejections of claims 1-15 are improper and Applicant requests that they be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections/objections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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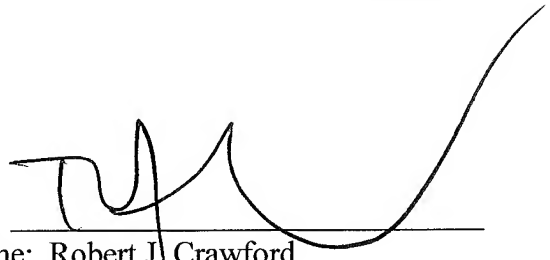
By: 
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